## IN THE CLAIMS

**This listing of claims will replace all prior versions, and listings, of the claims:**

1. (Currently Amended) A computer system comprising:

a processor;

a first bus coupled to the processor;

~~a memory controller coupled to the first bus;~~

a memory ~~coupled to the memory controller~~;

~~a first input/output (I/O) controller coupled to the first bus;~~ and

a core electronics complex including:

a memory controller coupled to the first bus and the memory;

a first input/output (I/O) controller coupled to the first bus; and

a test module coupled to the first I/O controller;

wherein the test module is configured to cause tests to be performed on the memory using the first bus.

2. (Original) The computer system of claim 1 further comprising:

an operating system;

wherein the processor is configured to cause the operating system to be booted, and wherein the test module is configured to cause the tests to be performed on the memory using the first bus subsequent to the operating system being booted.

3. (Original) The computer system of claim 1 further comprising:

an operating system;

wherein the processor is configured to cause the operating system to be executed, and wherein the test module is configured to cause the tests to be performed on the memory using the first bus during execution of the operating system.

4. (Original) The computer system of claim 1 wherein the first bus comprises a system bus.

5. (Currently Amended) The computer system of claim 1 further comprising:

~~a second I/O controller coupled to the first bus;~~

a second bus~~ coupled to the second I/O controller~~; and

a device coupled to the second bus;

wherein the core electronics complex includes a second I/O controller coupled to the first bus and the second bus.

6. (Original) The computer system of claim 1 wherein the test module is configured to cause tests to be performed on the memory using the first bus by providing read and write transactions to the first I/O controller.

7. (Original) The computer system of claim 6 wherein the read and write transactions comprise direct memory access (DMA) transactions.

8. (Original) The computer system of claim 1 further comprising:

a bus bridge coupled to the first bus and the first I/O controller.

9. (Currently Amended) A method performed by a computer system that includes a memory comprising:

selecting a portion of the memory for testing during operation of the computer system;

generating a test transaction in a test module coupled to an input/output (I/O) controller, the test module and the I/O controller included in a chipset coupled to the memory; and

providing the test transaction to the portion using direct memory access (DMA).

10. (Original) The method of claim 9 further comprising:

detecting an error that occurs in response to the test transaction; and

performing a remedial action in response to detecting the error.

11. (Currently Amended) The method of claim 9 further comprising:

providing the test transaction from the test module to the I/O controller;

providing the test transaction from the I/O controller to a bus bridge included in the chipset;

providing the test transaction from the bus bridge to a system bus;

providing the test transaction from the system bus to a memory controller; and

providing the test transaction from the memory controller to the portion.

12. (Original) The method of claim 11 further comprising:

storing information in the memory in response to the test transaction being a write transaction.

13. (Original) The method of claim 11 further comprising:

in response to the test transaction being a read transaction:

providing information associated with the test transaction from the portion to the memory controller;

providing the information from the memory controller to the system bus;

providing the information from the system bus to the bus bridge;

providing the information from the bus bridge to the I/O controller; and

providing the information from the I/O controller to the test module.

14. (Currently Amended) The method of claim 9 further comprising:

providing the test transaction from the test module to the I/O controller;

providing the test transaction from the I/O controller to a system controller included in the chipset;

providing the test transaction from the system controller to a memory controller; and

providing the test transaction from the memory controller to the portion.

15. (Currently Amended) A computer system comprising:

a processor;

a bus coupled to the processor;

~~a system controller coupled to the bus;~~

a memory ~~coupled to the system controller~~;

a core electronics complex including:

a system controller coupled to the bus and the memory;

an input /output (I/O) controller coupled to the system controller; and

a test module coupled to the I/O controller;

wherein the test module is configured to cause tests to be performed on the memory using direct memory access (DMA).

16. (Original) The computer system of claim 15 further comprising:

an operating system;

wherein the processor is configured to cause the operating system to be booted, and wherein the test module is configured to cause the tests to be performed on the memory using DMA subsequent to the operating system being booted.

17. (Original) The computer system of claim 15 further comprising:

an operating system;

wherein the processor is configured to cause the operating system to be executed, and wherein the test module is configured to cause the tests to be performed on the memory using DMA during execution of the operating system.

18. (Original) The computer system of claim 15 wherein the bus comprises a system bus.

19. (Original) The computer system of claim 15 wherein the test module is configured to cause tests to be performed on the memory using DMA by providing read and write transactions to the I/O controller.

20. (Original) The computer system of claim 19 wherein the read and write transactions comprise direct memory access (DMA) transactions.